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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,928	10/20/2003	Krisztian Flautner	550-465	8328

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EXAMINER	
CHERRY, STEPHEN J	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,928	FLAUTNER ET AL.	
	Examiner	Art Unit	
	Stephen J. Cherry	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-25-04, 9-16-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in United Kingdom on 11-12-2002, 12-6-2002, and 3-10-2003. It is noted, however, that applicant has not filed a certified copy of the 0226395.2, 0228546.8, and 0305442.6 applications as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims merely set forth steps of manipulating information and measured values and do not produce a tangible result. Additionally, claims 14-26 are directed to a computer program product, but do not recite a computer readable medium; therefore, the scope of the claims includes functional descriptive material which is not patentable. Although claims 27-39 are directed to an apparatus, the claim limitations set forth functional language that does not produce a tangible result; therefore they are non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Flautner and Mudge, "Vertigo: Automatic Performance-Setting for Linux" (vertigo).

Regarding claim 1, Flautner and Mudge disclose in Vertigo a method of calculating a target processor performance level of a processor from a utilisation history of said processor in performance of a plurality of processing tasks, said method comprising the steps of:

calculating a task work value indicating processor utilisation in performing a given processing task within a predetermined task time-interval (vertigo, eq. 4. "work estimate"); and

calculating said target processor performance level in dependence upon said task work value (vertigo, eq. 4. "perf").

Regarding claim 2, and in view of the rejection of claim 1, Flautner and Mudge disclose in Vertigo a method as claimed in claim 1, comprising calculating a plurality of task work values corresponding to a respective plurality of previous executions of said given processing task and combining said plurality of task work values to calculate said target processor performance level for a future execution of said given processing task (vertigo, page 6, line 21).

Regarding claim 3, and in view of the rejection of claim 2, Flautner and Mudge disclose in Vertigo a method as claimed in claim 2, wherein said predetermined task time-interval is independently set for each of said plurality of processing tasks (vertigo, fig. 5, related to particular episode, and page 6, line 21).

Regarding claim 4, and in view of the rejection of claim 3, Flautner and Mudge disclose in Vertigo a method as claimed in claim 3, wherein said predetermined task time-interval is independently set for each execution of said given processing task (vertigo, fig. 5, time depicted under "particular performance level" for particular episode, and page 6, line 21).

Regarding claim 5, and in view of the rejection of claim 4, Flautner and Mudge disclose in Vertigo a method as claimed in claim 4, wherein said predetermined task time-interval is a time period extending from the start of a first scheduling of said given processing task to the start of a subsequent scheduling of said given processing task, said predetermined task time-interval being associated with said first scheduling (vertigo, page 6, line 12).

Regarding claim 6, and in view of the rejection of claim 2, Flautner and Mudge disclose in Vertigo a method as claimed in claim 2, wherein said plurality of task work values corresponding to previous executions of said given processing task are

combined to calculate an exponentially decaying average work done value for said given processing task (vertigo, page 6, line 30).

Regarding claim 7, and in view of the rejection of claim 1, Flautner and Mudge disclose in Vertigo a method as claimed in claim 1, comprising detecting an idle time duration value within said predetermined task time-interval and calculating a task execution deadline for said given processing task in dependence upon said task work value and said idle time duration (vertigo, fig. 4, and page 5, line 8).

Regarding claim 8, and in view of the rejection of claim 7, Flautner and Mudge disclose in Vertigo a method as claimed in claim 7, wherein said task execution deadline is calculated for each of a plurality of previous executions of said given processing task and the plurality of task execution deadlines are combined to calculate an exponentially decaying average task execution deadline value (vertigo, page 6, line 30).

Regarding claim 9, and in view of the rejection of claim 7, Flautner and Mudge disclose in Vertigo a method as claimed in claim 7, wherein said target processor performance level for said given processing task is calculated in dependence upon said exponentially decaying average work done value and said exponentially decaying average task execution deadline value corresponding to said given processing task (vertigo, page 6, line 30).

Regarding claim 10, and in view of the rejection of claim 1, Flautner and Mudge disclose in Vertigo a method as claimed in claim 1 further comprising the steps of:

detecting at least one suspended execution period during processing of said given processing task, said at least one suspended execution period representing a time period during which processing is switched from said given processing task to a further, different processing task prior to completion of said first task (vertigo, page 5, line 3); and

calculating said task work value for said given processing task such that it includes processor utilisation during said at least one suspended execution period (vertigo, page 5, line 7).

Regarding claim 11, and in view of the rejection of claim 10, Flautner and Mudge disclose in Vertigo a method as claimed in claim 10, comprising setting an upper threshold for said predetermined task time-interval such that if said given processing task continues to execute without detection of said suspended execution period for a duration greater than or equal to said upper threshold, said target processor performance level for said task is automatically recalculated (vertigo, page 6, line 37).

Regarding claim 12, and in view of the rejection of claim 1, Flautner and Mudge disclose in Vertigo a method according to claim 1, wherein a flag value is stored for

each task, said flag value: indicating if the corresponding task has started to execute but has not yet completed execution (vertigo, page 5, line 12, "run bit").

Regarding claim 13, and in view of the rejection of claim 2, Flautner and Mudge disclose in Vertigo a method as claimed in claim 2, wherein each task work value for a respective previous execution of said given processing task is normalised by a corresponding predetermined task time-interval when combining said task work values to calculate said target processor performance level for said future execution of said task (vertigo, equations 2-4).

Regarding claim 14, Flautner and Mudge disclose in Vertigo a computer program product bearing a computer program for controlling a computer to calculate a target processor performance level of a processor from a utilisation history of said processor in performance of a plurality of processing tasks, said computer program comprising:

task work value calculating code operable to calculate a task work value indicating processor utilisation in performing a given processing task within a predetermined task time-interval (vertigo, eq. 4. "work estimate"); and

target processor performance calculating code operable to calculate said target processor performance level in dependence upon said task work value (vertigo, eq. 4. "perf").

Regarding claim 15, and in view of the rejection of claim 14, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 14, wherein said task work calculating code calculates a plurality of task work values corresponding to a respective plurality of previous executions of said given processing task and combining said plurality of task work values to calculate said target processor performance level for a future execution of said given processing task (vertigo, page 6, line 21).

Regarding claim 16, and in view of the rejection of claim 15, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 15, wherein said predetermined task time-interval is independently set for each of said plurality of processing tasks (vertigo, fig. 5, related to particular episode, and page 6, line 21).

Regarding claim 17, and in view of the rejection of claim 16, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 16, wherein said predetermined task time-interval is independently set for each execution of said given processing task (vertigo, fig. 5, time depicted under "particular performance level" for particular episode, and page 6, line 21).

Regarding claim 18, and in view of the rejection of claim 17, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 17, wherein said predetermined task time-interval is a time period ectending from the start of a first scheduling of said given processing task to the start of a subsequent scheduling of said

given processing task, said predetermined task time-interval being associated with said first scheduling (vertigo, page 6, line 12).

Regarding claim 19, and in view of the rejection of claim 15, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 15, wherein said plurality of task work values corresponding to previous executions of said given processing task are combined to calculate an exponentially decaying average work done value for said given processing task (vertigo, page 6, line 30).

Regarding claim 20, and in view of the rejection of claim 14, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 14, comprising detecting code operable to detecting an idle time duration value within said predetermined task time-interval and calculating a task execution deadline for said given processing task in dependence upon said task work value and said idle time duration (vertigo, fig. 4, and page 5, line 8).

Regarding claim 21, and in view of the rejection of claim 20, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 20, wherein said task execution deadline is calculated for each of a plurality of previous executions of said given processing task and the plurality of task execution deadlines are combined to calculate an exponentially decaying average task execution deadline value (vertigo, page 6, line 30).

Regarding claim 22, and in view of the rejection of claim 20, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 20, wherein said target processor performance level for said given processing task is calculated in dependence upon said exponentially decaying average work done value and said exponentially decaying average task execution deadline value corresponding to said given processing task (vertigo, page 6, line 30).

Regarding claim 23, and in view of the rejection of claim 14, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 14, further comprising:

suspended execution period detecting code operable to detect at least one suspended execution period during processing of said given processing task, said at least one suspended execution period representing a time period during which processing is switched from said given processing task to a further, different processing task prior to completion of said first task (vertigo, page 5, line 3); and

wherein said task work value calculating code is operable to calculate said task work value for said given processing task such that it includes processor utilisation during said at least one suspended execution period (vertigo, page 5, line 7).

Regarding claim 24, and in view of the rejection of claim 23, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 23, wherein an upper threshold for said predetermined task time-interval is set such that if said given processing task continues to execute without detection of said suspended execution period for a duration greater than or equal to said upper threshold, said target processor performance level for said task is automatically recalculated (vertigo, page 6, line 37).

Regarding claim 25, and in view of the rejection of claim 14, Flautner and Mudge disclose in Vertigo a computer program product according to claim 14, wherein a flag value is stored for each task, said flag value indicating if the corresponding task has started to execute but has not yet completed execution (vertigo, page 5, line 12, "run bit").

Regarding claim 26, and in view of the rejection of claim 15, Flautner and Mudge disclose in Vertigo a computer program product as claimed in claim 15, wherein each task work value for a respective previous execution of said given processing task is normalised by a corresponding predetermined task time-interval when combining said task work values to calculate said target processor performance level for said future execution of said task (vertigo, equations 2-4).

Regarding claim 27, Flautner and Mudge disclose in Vertigo an apparatus for calculating a target processor performance level of a processor from a utilisation history of said processor in performance of a plurality of processing tasks, said apparatus comprising:

task work value calculating logic operable to calculate a task work value indicating processor utilisation in performing a given processing task within a predetermined task time-interval (vertigo, eq. 4. "work estimate"); and

target processor performance calculating logic operable to calculate said target processor performance level in dependence upon said task work value (vertigo, eq. 4. "perf").

Regarding claim 28, and in view of the rejection of claim 27, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 27, wherein said task work calculating logic calculates a plurality of task work values corresponding to a respective plurality of previous executions of said given processing task and combining said plurality of task work values to calculate said target processor performance level for a future execution of said given processing task (vertigo, page 6, line 21).

Regarding claim 29, and in view of the rejection of claim 28, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 28, wherein said predetermined task time-interval is independently set for each of said plurality of processing tasks (vertigo, fig. 5, related to particular episode, and page 6, line 21).

Regarding claim 30, and in view of the rejection of claim 29, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 29, wherein said predetermined task time-interval is independently set for each execution of said given processing task (vertigo, fig. 5, time depicted under "particular performance level" for particular episode, and page 6, line 21).

Regarding claim 31, and in view of the rejection of claim 30, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 30, wherein said predetermined task time-interval is a time period extending from the start of a first scheduling of said given processing task to the start of a subsequent scheduling of said given processing task, said predetermined task time-interval being associated with said first scheduling (vertigo, page 6, line 12).

Regarding claim 32, and in view of the rejection of claim 28, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 28, wherein said plurality of task work values corresponding to previous executions of said given processing task are combined to calculate an exponentially decaying average work done value for said given processing task (vertigo, page 6, line 30).

Regarding claim 33, and in view of the rejection of claim 28, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 28, comprising detecting logic

operable to detecting an idle time duration value within said predetermined task time-interval and calculating a task execution deadline for said given processing task in dependence upon said task work value and said idle time duration (vertigo, fig. 4, and page 5, line 8).

Regarding claim 34, and in view of the rejection of claim 33, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 33, wherein said task execution deadline is calculated for each of a plurality of previous executions of said given processing task and the plurality of task execution deadlines are combined to calculate an exponentially decaying average task execution deadline value (vertigo, page 6, line 30).

Regarding claim 35, and in view of the rejection of claim 33, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 33, wherein said target processor performance level for said given processing task is calculated in dependence upon said exponentially decaying average work done value and said exponentially decaying average task execution deadline value corresponding to said given processing task (vertigo, page 6, line 30).

Regarding claim 36, and in view of the rejection of claim 28, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 28, further comprising:

suspended execution period detecting logic operable to detect at least one suspended execution period during processing of said given processing task, said at least one suspended execution period representing a time period during which processing is switched from said given processing task to a further, different processing task prior to completion of said first task (vertigo, page 5, line 3); and

wherein said task work value calculating logic is operable to calculate said task work value for said given processing task such that it includes processor utilisation during said at least one suspended execution period (vertigo, page 5, line 7).

Regarding claim 37, and in view of the rejection of claim 36, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 36, wherein an upper threshold for said predetermined task time-interval is set such that if said given processing task continues to execute without detection of said suspended execution period for a duration greater than or equal to said upper threshold, said target processor performance level for said task is automatically recalculated (vertigo, page 6, line 37).

Regarding claim 38, and in view of the rejection of claim 28, Flautner and Mudge disclose in Vertigo an apparatus according to claim 28, wherein a flag value is stored for each task, said flag value indicating if the corresponding task has started to execute but has not yet completed execution (vertigo, page 5, line 12, "run bit").

Regarding claim 39, and in view of the rejection of claim 28, Flautner and Mudge disclose in Vertigo an apparatus as claimed in claim 28, wherein each task work value for a respective previous execution of said given processing task is normalised by a corresponding predetermined task time-interval when combining said task work values to calculate said target processor performance level for said future execution of said task (vertigo, equations 2-4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen J. Cherry whose telephone number is (571) 272-2272. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJC

MICHAEL NGHIEM
PRIMARY EXAMINER